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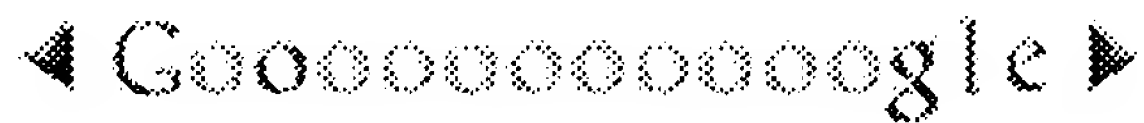www.chipkin.com/index.php/people/sss.php - 15k - Cached - Similar pages

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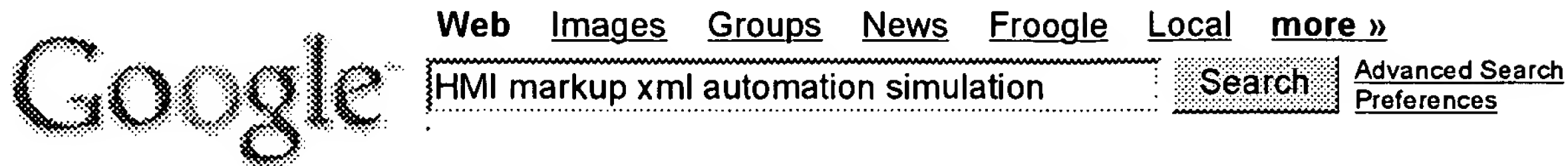Result Page: **Previous** 1 **2** 3 4 5 6 7 8 9 1011   **Next**

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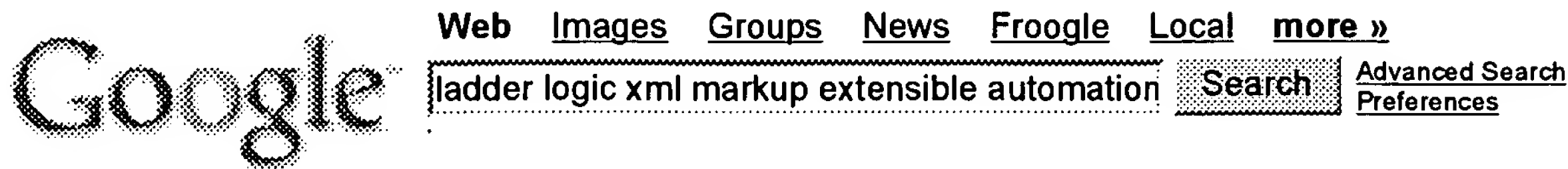**Free!** Google Desktop Search: Search your own computer. Download now.

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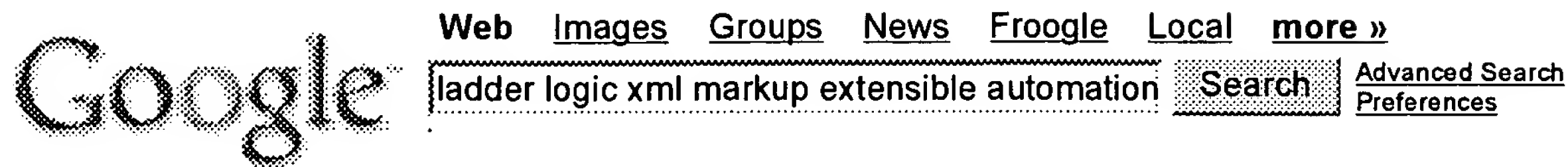www.control.com/960476284/index_html - 17k - Supplemental Result - <u>Cached</u> - <u>Similar pages</u>

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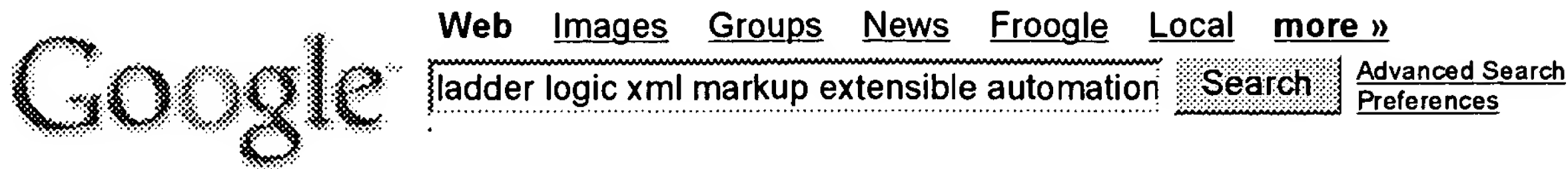Find: emails - files - chats - web history - media - PDF

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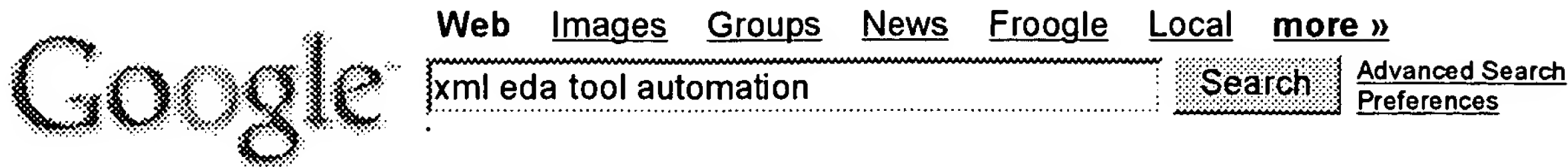Result Page: **Previous** 1 **2** 3 4 5 6 7 8 9 1011   **Next**

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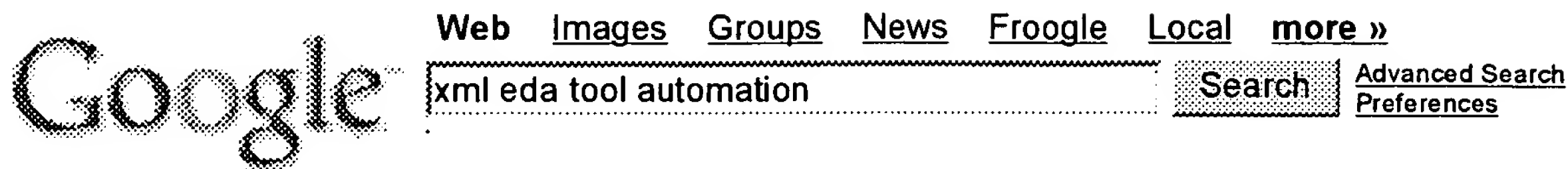| Google ▾ | | ▾ | Ⓖ Search ▾ | 🚫 | 📄 377 blocked | ꜟ Check ▾ | ⬝ AutoLink ▾ | AutoFill |

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which were originally developed for ATPG **tools**, play a key role in this development. Indirect
Design (ICCAD)pp. 538-543, 1993.
eda.ei.tum.de/pat/pat_dir/publications.html 18] P.
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<u>Yield Learning in Integrated Circuit Package Assembly - Balasubramaniam, Sarwar.. (1997)</u> <u>(Correct)</u>
assembly. The goal was to provide a management **tool** for making yield projections, resource
On Computers. research.cs.tamu.edu/**eda**/papers/sbala97.pdf
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M. Sarrafzadeh. DRAGON2000: Standard-cell placement **tool** for large industry circuits. In ICCAD, 2000. 16]
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<u>Wafer Signature Analysis of I DDQ Test Data - Sagar Sabade Walker</u> <u>(Correct)</u>
2002, pp. 47-52. research.cs.tamu.edu/**eda**/papers/dbt03.pdf
research.cs.tamu.edu/**eda**/pubs.htm Wafer Signature Analysis of I DDQ Test
research.cs.tamu.edu/eda/papers/dbt03.pdf

<u>Modeling and Optimization of VLSI Interconnects - He (1999)</u> <u>(Correct)</u>
University. Developed a fast-timing simulation **tool**, and a digital-analog mixed-mode SPICE. 1994
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<u>Using HOL to study Sugar 2.0 semantics - Gordon</u> <u>(Correct)</u>
mathematically sophisticated **tool** support for such **XML**-based representations. See the end of Section 5.4
required by systems, semiconductor and design **tools** companies, which enhance a language-based design
Regular Expressions. Sugar 2.0 1 www.**eda**.org/vfv/hm/ 2
www.cl.cam.ac.uk/~mjcg/Sugar/FinalCatBPaper.ps

<u>LPSAT: A Unified Approach to RTL Satisfiability - Zhihong Zeng Priyank (2001)</u> <u>(Correct)</u> <u>(3 citations)</u>
Can Greatly Impact The Performance Of Many **Eda Tools**. With Respect To Applications In Vlsi Cad, Most
applications in the electronic design automation (**EDA**) arena, including test pattern generation, timing
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www.sigda.org/Archives/ProceedingArchives/Date/Date2001/papers/2001/date01/htmfiles/sun_sgi/../../pdffiles/06c

<u>Accelerating Boolean Satisfiability through.. - Zhao, Malik.. (2001)</u> <u>(Correct)</u> <u>(1 citation)</u>
domains, especially in Electronic Design Automation (**EDA**) and Artificial Intelligence. In the **EDA** domain,
Automation (**EDA**) and Artificial Intelligence. In the **EDA** domain, SAT is embedded in many areas of design
www.capsl.udel.edu/COMPILER/ISSS01/isss01/papers/2001/isss01/pdffiles/p244.pdf

<u>A Parallel Interior-Point Algorithm for Linear Programming.. - Andersen, Andersen (1998)</u> <u>(Correct)</u> <u>(2 citations)</u>
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University, DK-5230 Odense M, Denmark. E-mail: **eda**@busieco.ou.dk. y CORE, Catholic University of

7:143-158, 1997. 30 www.kdaworld.com/**eda**/papers/paposlp.ps
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ATPG Using Fast Justification and Propagation on the.. - Paul Tafertshofer..   (Correct)
engine of [1]Using these algorithms our **tool** TIP outperforms the state-of-the-art in structural
Europe (DATE)pp. 526-530, Mar. 1999.
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Integrity-driven Power and Signal Network Codesign - Jinjun Xiong And   (Correct)
M. Sarrafzadeh. DRAGON2000: Standard-cell placement **tool** for large industry circuits. In ICCAD, pages
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1999. **eda**.ee.ucla.edu/pub/c42.pdf **eda**.ee.ucla.edu/pub/ Integrity-driven Power and
eda.ee.ucla.edu/pub/c42.pdf

Retiming for DSM with Area-Delay Trade-Offs and Delay Constraints - Tabbara (1999)   (Correct)   (1 citation)
becoming more important. System-level integration **tools** would have to solve complex optimization problems
been a lot of debate about the challenges that the **EDA** industry will face in the DSM era. In this
Complexity It is generally agreed, within the **EDA** community [1]that Deep SubMicron (DSM)
www-cad.eecs.berkeley.edu/HomePages/atabbara/publications/ms.pdf

Formulae and Applications of Interconnect Estimation - Considering Shield Insertion   (Correct)
multifactor data. New York: Wiley, 1980. **eda**.ee.ucla.edu/pub/iccad01_spr.pdf
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NCR: A Self-scaling, Self-calibrated Metric for I DDQ.. - Sagar Sabade Walker (2002)   (Correct)
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The Associative-Skew Clock Routing Problem - Chen, Kahng, Qu, Zelikovsky (1999)   (Correct)   (1 citation)
and bounded-skew formulations dominate current **EDA tools**, i.e.relative sink delays are constrained for
skew problem is easier to address within current **EDA** frameworks than useful-skew (skew-scheduling)
zero- and bounded-skew formulations dominate current **EDA tools**, i.e.relative sink delays are constrained
vlsicad.cs.ucla.edu/papers/conference/c101.ps

The VHDL Standard - Meersman (1994)   (Correct)
overview of activities, organizations and European **tool** efforts Author: C. Meersman, E2S n.v. ESA Contract
www.vlsivie.tuwien.ac.at/mike/VHDLReport.ps

Teaching Custom Integrated Circuit Design and Verification - Don Bouldin Adam   (Correct)
test circuitry that are compatible with the Cadence **tool**set and AMIS-0.6 micron process are described.
circuits using electronic design automation (**EDA**) software. Each individual is assigned a project
and a second window exercising the appropriate **EDA tool** needed for the design. These practices have
microsys6.engr.utk.edu/ece/mse03-bouldin.pdf

On Using Satisfiability-Based Pruning Techniques in.. - Vasco Manquinho Joao (2000)   (Correct)   (4 citations)
Covering problems are widely used as a modeling **tool** in Electronic Design Automation (**EDA**)Recent
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www.sigda.org/Archives/ProceedingArchives/Date/Date2000/papers/2000/date00/htmfiles/sun_sgi/../../pdffiles/05c

High-Level Area and Current Estimation - Fei Li Lei (2004)   (Correct)
and reduction by using commercial synthesis **tools** such as Design Compiler. In Section 2, we propose
Conf.pp. 383-388, June 1997. **eda**.ee.ucla.edu/pub/current_estimation.pdf
eda.ee.ucla.edu/pub/ 17] F. Li, L. He, J. Basile, R.
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Component Selection and Matching for IP-Based Design - Ting Zhang Stanford (2001)   (Correct)   (3 citations)

The system is based on Extensible Markup Language (**XML**) specification both for IP libraries (a repository
IP component selection: IP-based design flow needs **tools** to facilitate the process of selecting the
is part of the JavaCAD framework, an Internet-based **EDA tool** aimed at providing IP protection in
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An Architecture for a Secure Service Discovery Service - Czerwinski, Zhao, Hodes.. (1999) (Correct)
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and queries use the eXtensible Markup Language (**XML**) to encode such factors as cost, performance,
between components. This paper presents the **design** of the SDS, focusing on both the architecture of
Section 2 begins our discussion by describing the **design** concepts used in order to achieve our goals. The
daedalus.cs.berkeley.edu/publications/sds-mobicom99.ps.gz

Resource Description Framework (RDF) Model and Syntax.. - Lassila, Swick (1998) (Correct) (44 citations)
presented here uses the Extensible Markup Language [**XML**]one of the goals of RDF is to make it possible
www.dbis.informatik.hu-berlin.de/lehre/SS99/ecseminar/paper/thema3/WD-rdf-syntax-19981008.ps.gz

Virtualization of Course Structures through Adaptive Internet .. - Köppen, Neumann (1998) (Correct)
nestroy.wi-inf.uni-essen.de/Forschung/Publikationen/GfKl98a/Adaptiv.ps

Program Mobile Robots in Scheme - Rees, Donald (1992) (Correct) (8 citations)
IEEE International Conference on Robotics and **Automation**. 7] Erann Gat. ALFA: A language for
ffl Small physical size (one 10 by 17 by 1 cm **circuit** board) this means small memory size
space. Although the programming environment was **design**ed with one particular mobile robot architecture
ftp.cs.cornell.edu/pub/brd/scheme-mobile-robots.ps.Z

Systems Performance Measurement on PCI Pamette - Laurent Moll (1997) (Correct) (8 citations)
the PCI interface, and all can be reconfigured in **circuit**. This paper describes a collection of simple
the reconfigurable logic is seen as a coprocessor **design**ed to work in harmony with the host processor.
an exception. Therefore a significant part of the **design** effort in PCI Pamette has gone into understanding
ftp.digital.com/pub/DEC/SRC/publications/shand/fccm97.ps

A Control-Theoretic Approach to Flow Control - Keshav (1991) (Correct) (203 citations)
behalf of each conversation (also called channel, **circuit** or virtual **circuit** we use `conversation'
a continuous-time system model. This is used to **design** a variant of the control law that is also
technique (4)This is used as the basis for the **design** of a stable rate-based flow control scheme (5)
simon.cs.cornell.edu/Info/People/skeshav/tenet/Keshav91a.ps

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ftp.cs.buffalo.edu/pub/tech-reports/95-18.ps.Z

Programming Language Expressiveness and Circuit Complexity - Dancanet, Brookes (1996) (Correct)
Programming Language Expressiveness and **Circuit** Complexity Denis Dancanet Stephen Brookes
www.cs.cmu.edu/afs/cs.cmu.edu/user/ddr/www/mfps96.ps

Variation Fluctuation Smoothing for ATM Circuit Emulation.. - McDonald, Liao, Giroux (Correct)
Variation Fluctuation Smoothing for ATM **Circuit** Emulation Service David McDonald a Rui-Feng
www.uottawa.ca/~dmcdonal/papers/ces.ps

Pragmatic Issues in Handling Miscommunication: Observations of .. - Ronnie Smith (1996) (Correct)
(2 citations)
capable of variable initiative behavior, the **Circuit** FixIt Shop. In general, the 141 dialogs obtained
www.cs.ecu.edu/faculty/smith/www/papers/aaai96wrk.ps

Worlds To Die For - Hemaspaandra, Ramachandran, Zimand (1995)   (Correct)
function that is computable by polynomial-size **circuits** of depth i 1 but which cannot be computed by a
168.18.216.164/~zimand/papers/sigact.ps

A BDD-based Verification Engine for Combinational Equivalence.. - van Eijk (1997)   (Correct)
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equivalent signals and of isomorphic sub-**circuits**. Experimental results on well-known benchmarks
on well-known benchmarks as well as industrial **designs** are presented to evaluate these techniques.
www.stw.nl/prorisc/cssp97/proc/psz/eijk.ps.gz

Non-Heuristic Optimization and Synthesis of Parallel-Prefix.. - Reto Zimmermann (1996)   (Correct)   (3 citations)
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adders, non-heuristic synthesis algorithm, **circuit** timing and area optimization, computer
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www.iis.ee.ethz.ch/~zimmi/publications/adder_synthesis.ps.gz

Spectral Methods for Matrix Rigidity with Applications to.. - Satyanarayana Lokam (1995)   (Correct)   (1 citation)
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www.cs.utoronto.ca/~satya/focsversion.ps

Issues In Distributed Control For Atm Networks - Jonathan Turner (1995)   (Correct)   (1 citation)
antecedents (e.g. the telephone network, virtual **circuit** data networks) focuses on specific protocols and
of ATM networks and explores some of the key **design** issues through a series of examples. It is hoped
11, 12, 13, 15, 17, 21]Discussion of alternative **design** approaches and useful surveys are rare [20]This
www.cs.wustl.edu/cs/techreports/1995/wucs-95-12.ps.Z

Integrated Fault Diagnosis Targeting Reduced Simulation - Boppana, Fuchs (1996)   (Correct)
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D. Friedman, Digital Systems Testing and Testable **Design**, Computer Science Press, New York, 1990. 2] P.
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Efficient Signaling Algorithms for ATM Networks - Tan, Campbell   (Correct)
between two end-points occurs over a virtual **circuit**. All cells for the same conversation flow along
Interface signaling. In previous work, we **design**ed the GULP protocol as well as an architecture
other data and is an important feature of the **design**. Minimizing the number of rounds decreases the
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Hence, for this operation, it may be feasible to **design** a routing algorithm that requires a processor to
ringer.cs.utsa.edu/faculty/boppana/papers/USC90.ps

Diagnostic Simulation of Sequential Circuits Using Fault.. - Srikanth Venkataraman   (Correct)
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Terabit Burst Switching - Jonathan Turner (1997)   (Correct)   (65 citations)
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